Custom Operations

Sometimes custom program code must be run on the 4152-X.

The 4152-X comes standard with 64 KiB of addressable system memory. 32 KiB is reserved for System ROM to store the Runtime Environment. User Programs are limited to 46 bytes. Due to the non-deterministic nature of our patent-pending Quantum Loading Framework, we cannot document the many specific memory locations of System ROM or the user accessible RAM, as they are different every time. Therefore, we recommend not power cycling your device often, as this may complicate Programming and Debugging operations.

Registers

The CPU has 4 general purpose Data Registers, 2 user accessible Address Registers and 2 special use Streaming Registers.

Register Name	Symbol	Bytecode Equivalent
Data Register 0, Accumulator	DR0 (ACC)	0x00
Data Register 1	DR1	0x01
Data Register 2	DR2	0x02
Data Register 3	DR3	0x03
Address Register 0	AR0	0x04
Address Register 1	AR1	0x06
Streaming Register	SR0	0x08
Streaming Register Page Number	SR1	0x09

Operands

Working With Memory

Symbol, Usage	Description	Bytecode Equivalent
CPP <src, dst>	Copy page src to dst	0x01
CPPR <src, dst>	Copy page referenced by src register to dst	0x81
CPY <src, dst>	Copy value between registers	0x02
MOV <src, dst>	Same as CPY, but clears src	0x03
SWP <src, dst>	Swap the two listed registers	0x04

Flow Control

Symbol, Usage	Description	Bytecode Equivalent
LBL <val>	Set a label of val at the current location	0x05
LBC <val>	Set a label of val for the location specified by AR0	0x06
JMP <label>	Jump unconditionally to label	0x07
JEZ <label>	Jump if ACC = 0	0x08
JNZ <label>	Jump if ACC != 0	0x09
JPG <page>	Jump to the specified page	0x0A
RET	Jump to the location specified in AR0	0x0B

Working with Data

Symbol, Usage	Description	Bytecode Equivalent
LDA <val>	Load byte into DR0 (ACC)	0x0C
LDB <val>	Load byte into DR1	0x0D
LDC <val>	Load byte into DR2	0x0E
LDD <val>	Load byte into DR3	0x0F
LDR <val, dst>	Load byte into register	0x10
ASA <val page, val offset>	Set AR0 to 16 bit location	0x11
ASB <val page, val offset>	Set AR1 to 16 bit location	0x12
ALA <label>	Load location of label into AR0	0x13
ALB <label>	Load location of label into AR1	0x14
ADM <src, dst>	Dump high/low order bytes of the specified address register to dst register and dst+1	0x15
STR	Load memory range defined by AR0 (start) and AR1 (end) into the Streaming Register (SR0)	0x16
STA	Load next byte into the Streaming Register (SR0)	0x17

Manipulating Data

Symbol, Usage	Description	Bytecode Equivalent
INC <reg>	Increment the register by one. Overflows will not be carried, and the register will be set to 0.	0x18
DEC <reg>	Decrement the register by one. Underflows will be set to 0.	0x19
ADD <reg, val>	Add val to the register. Overflows will not be carried, and the register will be set to 0.	0x1A
SUB <reg, val>	Subtract val from the register. Underflows will be set to 0.	0x1B

Working With Data

Symbol, Usage	Description	Bytecode Equivalent
REQ <A, B>	Set ACC to 0x01 if registers A and B are equal, otherwise 0x00.	0x1C
RLT <A, B>	Set ACC to 0x01 if register A < B, otherwise 0x00	0x1D
RGT <A, B>	Set ACC to 0x01 if register A > B, otherwise 0x00	0x1E
RLE <A, B>	Set ACC to 0x01 if register A <= B, otherwise 0x00	0x1F
RGE <A, B>	Set ACC to 0x01 if register A >= B, otherwise 0x00	0x20

Bitwise Operations

Symbol, Usage	Description	Bytecode Equivalent
AND <A, B>	Set ACC to the logical AND of registers A and B	0x21
OR <A, B>	Set ACC to the logical OR of registers A and B	0x22
XOR <A, B>	Set ACC to the logical XOR of registers A and B	0x23

Special Operands

Symbol, Usage	Description	Bytecode Equivalent
PRN	Flush the print buffer to the printer. Calling this Operand will terminate the program.	0x24

Memory Layout

Address	Use
0xD000-0xFFFF	???
0xC000-0xCFFF	This is a static location assigned to the print buffer
0x0200-0xBFFF	???
0x0100-0x01FF	Page 1: Reserved for User Programs
0x0000-0x00FF	Page 0: System Reserved. This is where the CPU registers reside